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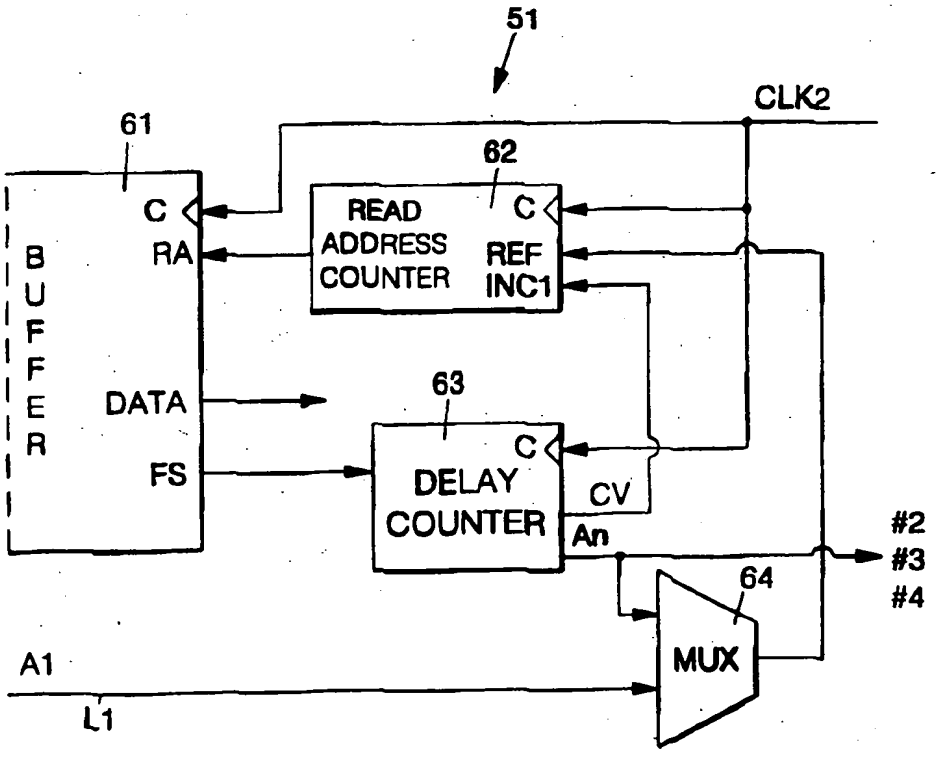
(54) Title: A METHOD AND A DEVICE FOR ALIGNING FRAMES OF SIGNALS TO BE USED IN A SYNCHRONOUS DIGITAL TELECOMMUNICATIONS SYSTEM

(57) Abstract

The invention relates to a method and a device for aligning frames of signals to be used in a synchronous digital telecommunications system with each other. In the method, bytes of the frames are stored in an elastic buffer (61). In order to provide an automatic and as simple as possible way of implementing the alignment, (a) a delay measurement is started at the same phase of the frame of each signal, (b) after a certain predetermined delay period, a reference signal (A1) is produced from the delay measurement concerning one signal to be aligned, and (c) from a value (CV) indicated by the delay measurement concerning each signal to be aligned at the moment of occurrence of said reference signal, a read address is generated for the respective signal to be aligned in said elastic buffer (61).



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A method and a device for aligning frames of signals to be used in a synchronous digital telecommunications system

The invention relates to a method for aligning frames of signals to be used in a synchronous digital telecommunications system, such as an SDH or SONET system, with each other, which signals have a frame structure comprising a predetermined number of bytes of constant length, in which method said bytes are stored in an elastic buffer.

The solution of the invention is especially intended for regenerators of a synchronous digital telecommunications system, but it can be applied to any network element of the system in principle, if there is a need to align two or several signals of the same hierarchy level with each other.

The current digital transmission network is plesiochronous, i.e. each 2 Mbit/s basic multiplex system has a dedicated clock independent of any other system. It is therefore impossible to locate a single 2 Mbit/s signal in the bit stream of a higher-order system, but to extract the 2 Mbit/s signal the higher-level signal has to be demultiplexed through each intermediate level down to the 2 Mbit/s level. For this reason, it has been expensive to construct especially branch connections requiring several multiplexers and demultiplexers. Another disadvantage of the plesiochronous transmission network is that equipments from two different manufacturers are usually not compatible.

The above drawbacks, among other things, have led to the definition of a new synchronous digital hierarchy SDH. The definition has been made in CCITT Recommendations G.707 to G.709 and G.781 to G.784, for instance. The synchronous digital hierarchy is based on

STM-N transfer frames (Synchronous Transport Modules) located on several levels of hierarchy N (N = 1, 4, 16...). Existing PCM systems, such as 2, 8 and 34 Mbit/s systems, are multiplexed into a synchronous 155.520 Mbit/s frame of the lowest level of the SDH (N=1), consistently with the above called the STM-1 frame. On the higher levels of hierarchy the bit rates are multiples of the bit rate of the lowest level. In principle, all nodes of the synchronous transmission network are synchronized into one clock. If some of the nodes should, however, lose connection with the common clock, it would lead to problems in the connections between the nodes. The phase of the frame must also be easy to recognize in the reception. For the reasons stated above, the SDH telecommunications have introduced a pointer, which is a number indicating the phase of the payload within the frame, i.e. the pointer indicates that byte in the STM frame from which the payload begins.

Figure 1 illustrates the structure of an STM-N frame, and Figure 2 a single STM-1 frame. The STM-N frame comprises a matrix with 9 rows and N x 270 columns so that there is one byte at the junction point between each row and column. Rows 1-3 and 5-9 of the N x 9 first columns comprise a section overhead SOH, and row 4 comprises an AU pointer. The rest of the frame structure is formed of a section having the length of N x 261 columns and containing the payload section of the STM-N frame.

Figure 2 illustrates a single STM-1 frame, one row of which is 270 bytes in length, as described above. The payload section comprises one or more administration units AU. In the example shown in the figure, the payload section consists of an administration unit AU-4, into which a corresponding virtual container VC-4 is inserted. (Alternatively, the STM-1 transfer frame may

contain three AU-3 units, each containing a corresponding virtual container VC-3). The VC-4 in turn consists of a path overhead POH located at the beginning of each row and having the length of one byte (9 bytes altogether), and of a payload section in which there are lower-level frames also comprising bytes allowing interface justification to be performed in connection with mapping when the rate of the information signal to be mapped deviates to some extent from its nominal value.

Each byte in the AU-4 unit has its own location number. The above-mentioned AU pointer contains the location of the first byte of the VC-4 container in the AU-4 unit. The pointers allow positive or negative pointer justifications to be performed at different points in the SDH network. If a virtual container having a certain clock frequency is applied to a network node operating at a clock frequency lower than the above-mentioned clock frequency of the virtual container, the data buffer will be filled up. This requires negative justification: one byte (3 bytes in case of a VC-4 container) is transferred from the received virtual container to the overhead section of the frame to be transmitted while the pointer value is correspondingly decreased by one. If the rate of the received virtual container is lower than the clock rate of the node, the data buffer tends to be emptied. Then a positive justification must be performed: a stuff byte (3 bytes in case of the VC-4 container) is added to the virtual container to be transmitted and the pointer value is incremented by one.

Figure 3 shows how an STM-N frame can be formed of existing bit streams. At the first stage, these bit streams (1.5, 2, 6, 8, 34, 45 or 140 Mbit/s, shown on the right in the figure) are packed into containers C specified by CCITT. At the second stage, overhead bytes

containing control data are inserted into the containers, whereby the above-described virtual container VC-11, VC-12, VC-2, VC-3 or VC-4 is obtained (the first suffix after the abbreviations represents the level of hierarchy and the second suffix represents the bit rate). This virtual container remains intact while it passes through the synchronous network up to its point of delivery. The virtual containers are further formed (depending on the level of hierarchy) either into so-called tributary units TU or into AU units (AU-3 and AU-4) mentioned above by providing them with pointers. The AU unit can be mapped directly into the STM-1 frame, whereas the TU units have to be assembled through tributary unit groups TUG and VC-3 and VC-4 units to form AU units, which can then be mapped into the STM-1 frame. In Figure 3, the mapping is indicated by a continuous thin line, the aligning with a broken line, and the multiplexing with a continuous thicker line.

As can be seen from Figure 3, the STM-1 frame may be assembled in a number of alternative ways, and the contents of the highest-level virtual container VC-4, for instance, may vary, depending on the level from which the assembly has been started and in which way the assembly has been performed. The STM-1 signal may thus contain e.g. 3 TU-3 units or 21 TU-2 units or 63 TU-12 units, or a combination of some of the above-mentioned units. As the higher-level unit contains several lower-level units, e.g. the VC-4 unit contains TU-12 units (there are 63 such units in a single VC-4 unit, cf. Figure 3), the lower-level units are mapped into the higher-level frame by interleaving so that the first bytes are first taken consecutively from each lower-level unit, then the second bytes, etc. The example of Figure 2 shows how the VC-4 unit contains at first con-

secutively the first bytes of all 63 TU-12 units, then the second bytes of all 63 TU-12 units, etc.

Since the above-described SDH frame structures and the assembly of such structures do not belong to the scope of the actual inventive idea, they will not be described more in this connection. The SDH frame structure and the assemble thereof are described e.g. in References [1] and [2], which are referred to for a more detailed description (the references are listed at the end of the specification).

Several signals of the same hierarchy level are usually aligned with each other (cf. Figure 3) by pointer operations, but in regenerators, for instance, pointer operations are not allowed, only a regenerator section overhead RSOH of a STM-1 frame can be processed therein. In case pointer operations cannot be used for the aligning, the aligning could be performed as a solution of shift register type, for instance, by adjusting delays in different signals. In such a solution, however, quite strict demands are made on tolerances of clock signal properties, such as fading.

The object of the present invention is to provide a method and a device, which do not require much of the clock signal to be used and by means of which signals of the same hierarchy level can be aligned with each other automatically in the simplest possible manner, i.e. without a necessity of monitoring the phase of an outgoing and incoming signal all the time. This object is achieved by means of the method and the device according to the invention, the method being characterized in that

- a delay measurement is started at the same phase of the frame of each signal,

- after a certain predetermined delay period, a reference signal is produced from the delay measurement concerning one signal to be aligned,

- from a value indicated by the delay measurement concerning each signal to be aligned at the moment of occurrence of said reference signal, a read address for the respective signal to be aligned is generated for said elastic buffer.

The device, in turn, is characterized in that it comprises

- time measurement means relating to each signal to be aligned for starting a delay measurement at a certain phase of the frame of each signal to be aligned, at least one of these means comprising pulse generating means for producing a reference pulse after a predetermined delay period, and

- address generating means relating to each signal to be aligned for generating a read address relating to each signal to be aligned for the elastic buffer from the value indicated by the delay measurement concerning said signal at the moment of occurrence of said reference pulse.

The idea of the invention is to adjust the storing time of each signal in a buffer on the basis of phase differences indicated by a delay measurement to be started at a certain phase of a frame for the purpose of aligning the signals with each other. Though the adjustment is made in steps determined by one cycle of a reading clock signal, the storing time is not tied to whole clock cycles, however, since the phase of a write clock may slide with respect to the read clock.

In the following, the invention and preferred embodiments thereof will be described in greater detail referring to the examples of the attached drawings according to the attached figures 4 to 6, in which

Figure 1 shows a basic structure of one STM-N frame,

Figure 2 shows the structure of one STM-1 frame,

Figure 3 shows an assembly of an STM-N frame of existing PCM systems,

Figure 4 shows a block diagram of an STM-4 node of a synchronous digital telecommunications system,

Figure 5 illustrates an aligning circuitry of an STM-4 unit shown in Figure 4, and

Figure 6 illustrates a more detailed block diagram of one aligning circuit shown in Figure 5.

Figure 4 shows an STM-4 node of an SDH network, the node comprising several parallel interface units 41, each of which receives (first transmission direction) an STM-1 signal coming from a fibre 42 and transmits (second transmission direction) the STM-1 signal to the fibre. In an STM-4 unit 43, an STM-4 signal is assembled of the received STM-1 signals for a fibre 44 and, correspondingly, from the STM-4 signal coming from the fibre 44 are disassembled four STM-1 signals for the fibres 42. Said first transmission direction is studied in this description.

An interface unit 41 changes the STM-1 signals into an electric form and transmits them further through an internal bus B of the node to the STM-4 unit 43, which assembles them further to an STM-4 signal. In such a situation, a problem arises from delays in the internal bus B, which are unequal for each STM-1 signal. Accordingly, though the interface units transmit the STM-1 signals to the bus (usually implemented on a back plane of the device) at the same edge of the clock signal, they arrive in the STM-4 unit at slightly different moments. (This is partly due to different transit delays of said clock signal to separate interface units.)

On account of the transit time differences referred to above, an alignment of the frames of incoming STM-1 signals has to be performed in the STM-4 unit 43. This is carried out by means of an aligning circuitry 50 according to the invention shown in Figure 5, the circuitry comprising four parallel aligning circuits 51 separated from each other in the figure by numbering them by reference marks #1 to #4. To each aligning circuit is brought from an interface circuit an STM-1 payload signal D, a frame synchronization signal FS and a clock signal CLK1. For the alignment, one of the aligning circuits 51, in this case circuit number 1, produces after a delay period measured from a certain phase of the frame a reference pulse A1, the moment of occurrence of which is used as a reference with respect to the other aligning circuits (#2 to #4), on the basis of which reference the alignment is performed. For this purpose, the reference signal A1 produced by the aligning circuit #1 is connected to all other aligning circuits 51. Due to the different position of the aligning circuit #1, it is called below a master circuit and the other aligning circuits (#2 to #4) are called slave circuits.

After the STM-1 signals have been aligned in the input of the STM-4 unit 43 in the manner according to the invention, the data is connected further to pointer generating and multiplexing circuits of the STM-4 unit for producing an STM-4 signal from four STM-1 signals by byte interleaving in a manner known per se. This does not, however, belong to the scope of the inventive idea any longer, and therefore, these circuits are not described in this connection.

Figure 6 illustrates a block diagram of the structure of one aligning circuit 51 in greater detail. The aligning circuit comprises an elastic buffer 61,

only the output side (read side) of which is shown in Figure 6, a read address counter 62 for giving a read address to the elastic buffer, a delay counter 63 measuring the delay from a certain phase of the frame and capable of adjusting the read address, as well as a multiplexer 64 selecting the right signal for the read address counter 62 in each aligning circuit.

In the aligning circuit 51, the incoming data D is written in the elastic buffer 61, from which it is read further by means shown in Figure 6. Except for data, the information of the phase of the frame is stored in the buffer. This signal is indicated by reference mark FS in the figure and it may indicate any point of the frame in principle, if only this point is identical for all signals to be aligned.

The synchronization pulse FS starts an aligning process according to the invention in each aligning circuit by starting the delay counter 63 while it is read (together with data) out of the buffer 61. After a predetermined delay period, when the delay counter 63 has achieved the predetermined reading, the delay counter produces a reference pulse An (n = 1, 2, 3 or 4) in its first output. In the master circuit (n = 1), this reference pulse A1 is led via the multiplexer 64 to a first input REF of the read address counter 62. Accordingly, in the master circuit the multiplexer 64 has selected the branch coming from the delay counter 63. Additionally, the reference pulse A1 of the master circuit is led to the other aligning circuits (#2 to #4), as shown in Figure 5.

At the moment of occurrence of the reference pulse A1, an increment value of the read address is obtained from a reading CV of the delay counter 63. This value is loaded at the rising edge of a clock signal CLK2 next to the moment of occurrence in question from

the second output of the delay counter to an input INC1 of the read address counter 62 for adjusting an increment step of the read address counter. The new read address to be connected to a read address input RA of the elastic buffer will be the previous address value added by the value CV the delay counter has at the moment of occurrence of the reference pulse A1 (value CV may also be negative, in which case it is a decrement value, respectively).

For providing a solution as simple as possible, it is preferable that the delay counter produces a reference pulse when its reading CV is +1. Since in the master circuit the reference pulse is supplied back to the read address counter of the same circuit, the read address counter of the master circuit steps normally also in this case (an increment step having the size of one unit).

By means of the other aligning circuits (so-called slave circuits #2 to #4), a signal received by means of the multiplexer 64 from an input line L1 is selected to the output of the multiplexer. To this input line is connected the reference signal A1 coming from the master circuit, which signal is connected to the reference input REF of the read address counter 62 of the aligning circuit. Then, the delay counter value CV obtained as an increment/decrement value of the read address counter at the moment of the reference pulse deviates from the increment value of the master circuit according to the phase difference between the respective STM signals. Consequently, by means of the increment/decrement value given by the delay counter, the mutual time period between writing in the elastic buffer and reading from the elastic buffer is adjusted (i.e. the length of the time is adjusted during which the data is stored in the elastic buffer). In this manner, the phase

of each signal can be adjusted with respect to the phase of the master circuit signal so that the frames of all signals will be aligned with respect to each other (in the same phase). Additionally, it shall be noted that the alignment occurs automatically, in the manner described above, once during a frame, started by the frame synchronization signal FS, and that the read address counter counts in other respects normally forward (the increment step being +1) at the rising edges of a clock signal CLK2 connected to its clock input C (i.e. reading from the buffer takes place normally during the other bytes of the frame).

The aligning circuits are described above as identical as possible. It would, of course, be possible to construct the master circuit so as to differ more clearly from the slave circuits, in which case there would be no multiplexer at all and only the slave circuits would have an input line L1, for instance. However, the above embodiment is preferable as to the fact that the master circuit and the slave circuits therein differ from each other only as far as the connection of the reference pulse and the control of the multiplexer are concerned. Thus, even if the delay counters of the slave circuits give a reference pulse after having reached a certain predetermined value, these reference pulses are not connected operatively to anything at all.

The delay counters 63 may be e.g. four-bit counters counting downwards, the counting area of which is such that the above-mentioned value +1 occurs approximately in the middle of the counting area (e.g. counting area 7,6...0, -1, -2...-7). It is naturally preferable to use the value +1 as the delay counter value corresponding to the moment of occurrence of the reference pulse, since it corresponds to the normal increment value of the read address counter. On the other hand,

it is preferable that the value +1 occurs approximately in the middle of the counting area, because the signals of the slave circuits may either lead or lag the signal of the master circuit. For example, if the above counting area is used and the delay counter value of the slave circuit is one of the values 7,6...2, the signal of the slave circuit lags the signal of the master circuit, due to which reading and writing said signal shall be adjusted temporally closer to each other. Correspondingly, if the delay counter value of the slave circuit is one of the values 0 to -7, the signal of the slave circuit leads the signal of the master circuit, due to which reading and writing said signal shall be adjusted temporally further off from each other. After the alignment, the value +1 is obtained from all delay counters at the moment of occurrence of the reference pulse.

Though the invention has above been described with reference to examples according to the attached drawings, it is clear that the invention is not restricted thereto, but it can be modified within the scope of the inventive idea set forth above and in the attached claims. Even if the invention has above been described as an example relating expressly to an SDH system, the solution of the invention can naturally be applied to any corresponding system, e.g. to a SONET system. Though the invention has further been described with reference to a signal on STM-1 level, it is clear that the invention can be applied to aligning signals on any hierarchy level.

List of references cited:

[1]. CCITT Blue Book, Recommendation G.709: "Synchronous Multiplexing Structure", May 1990.

[2]. SDH - Ny digital hierarki, TELE 2/90.

Claims:

1. A method for aligning frames of signals to be used in a synchronous digital telecommunications system, such as an SDH or SONET system, with each other, which signals have a frame structure comprising a predetermined number of bytes of constant length, in which method said bytes are stored in an elastic buffer (61), c h a r a c t e r i z e d in that

- a delay measurement is started at the same phase of the frame of each signal,

- after a certain predetermined delay period, a reference signal (A1) is produced from the delay measurement concerning one signal to be aligned,

- from a value (CV) indicated by the delay measurement concerning each signal to be aligned at the moment of occurrence of said reference signal, a read address for the respective signal to be aligned is generated for said elastic buffer (61).

2. A method according to claim 1, c h a r a c t e r i z e d in that the delay measurement is carried out by means of a delay counter (63), which is started at the same phase of the frame of each signal.

3. A method according to claim 2, c h a r a c t e r i z e d in that read addresses are generated by means of a counter (62) by incrementing/decrementing the counter with a value depending on the value (CV) of the delay counter (63) at the moment of occurrence of the reference signal.

4. A method according to claim 3, c h a r a c t e r i z e d in that the value of the delay counter (63) at the moment of occurrence of the reference signal is used directly as the increment/decrement value of the read address counter.

5. A method according to claim 2, c h a r -

a c t e r i z e d in that said reference pulse (A1) is produced substantially in the middle of the counting area of the delay counter (63).

6. A device for aligning frames of signals to be used in a synchronous digital telecommunications system, such as an SDH or SONET system, with each other, which signals have a frame structure comprising a predetermined number of bytes of constant length, which device comprises an elastic buffer (61) for storing signals and a read address counter (62) for each signal to be aligned for generating a read address for said elastic buffer (61) for reading said signal from the buffer (61), c h a r a c t e r i z e d in that it further comprises

- time measurement means (63) relating to each signal to be aligned for starting a delay measurement at a certain phase of the frame of each signal to be aligned, at least one of these means comprising pulse generating means (63) for producing a reference pulse (A1) after a predetermined delay period, and

- address generating means (62) relating to each signal to be aligned for generating a read address relating to each signal to be aligned for the elastic buffer (61) from the value (CV) indicated by the delay measurement concerning said signal at the moment of occurrence of said reference pulse (A1).

7. A device according to claim 6, c h a r a c t e r i z e d in that the time measurement means comprise a delay counter (63), whereby the first output of one delay counter is connected to said address generating means for producing the reference pulse (A1) for the address generation relating to each signal.

8. A device according to claim 7, c h a r a c t e r i z e d in that the address generating means comprise an address counter (62), to which the second

output of said delay counter (63) is operatively connected for giving the address counter (62) an increment/decrement value.

9. A device according to claim 8, characterized in that the first output of said one delay counter is connected to each address counter (62) via a multiplexer (64).

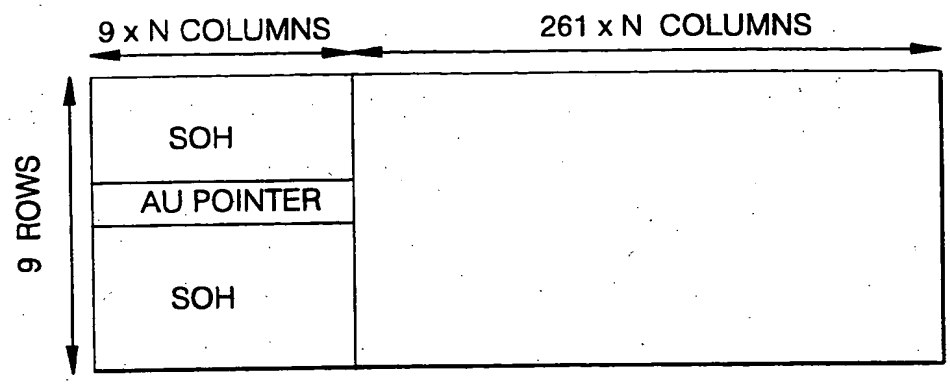
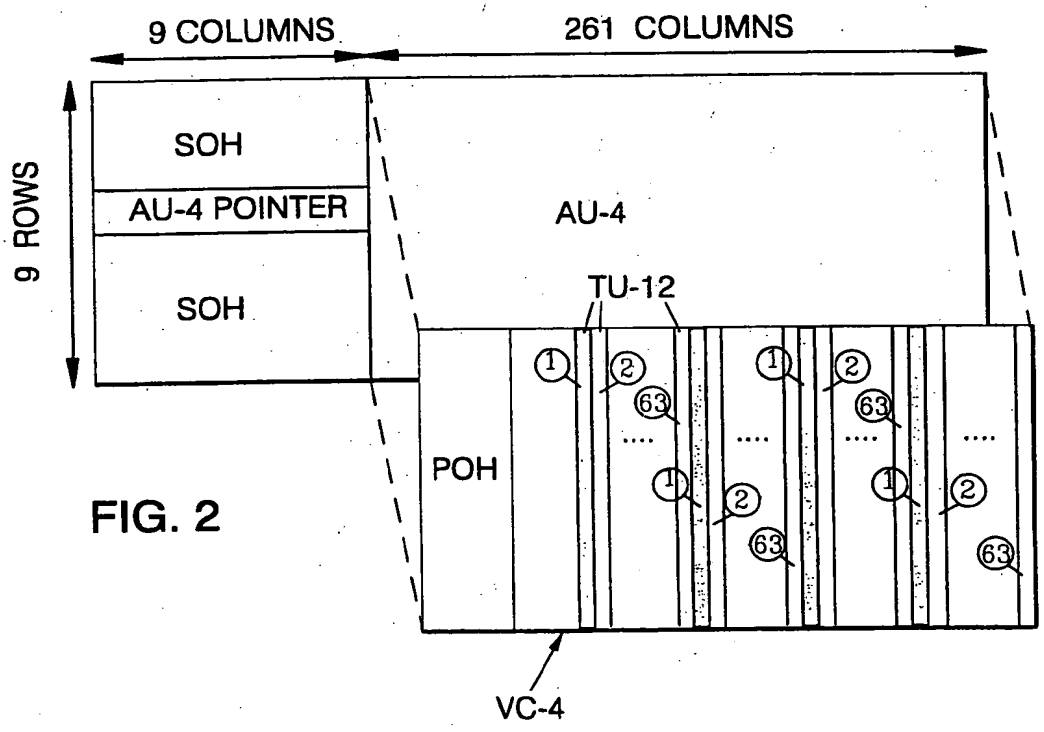

9 x N COLUMNS
261 x N COLUMNS
9 ROWS
SOH
AU POINTER
SOH

FIG. 1


9 COLUMNS
261 COLUMNS
9 ROWS
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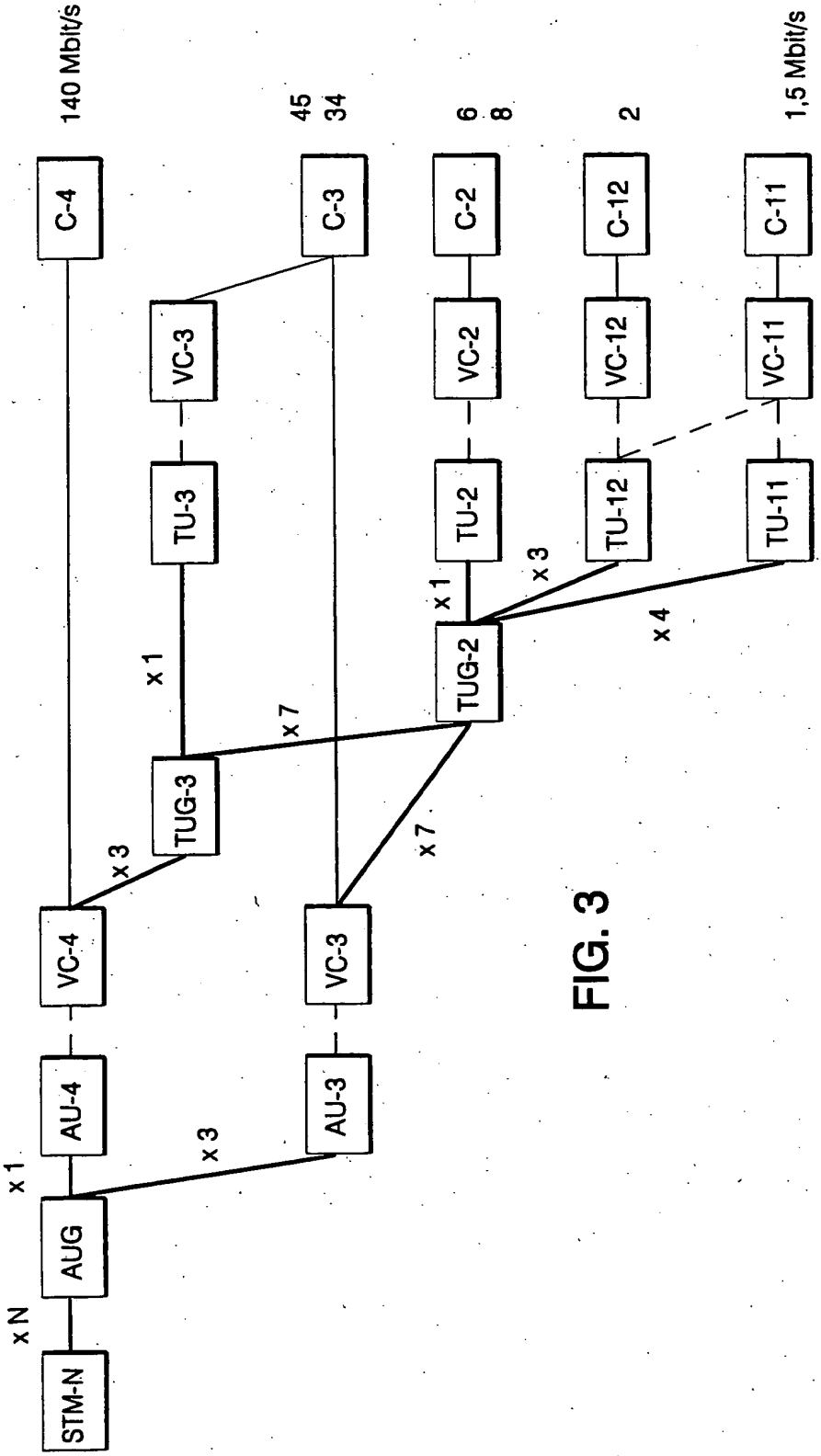
AU-4 POINTER
SOH
AU-4
TU-12
POH
1
2
63
VC-4

FIG. 2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45
34
6
8
2
1,5 Mbit/s
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C-3
C-2
C-12
C-11
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VC-12
VC-11
TU-3
TU-2
TU-12
TU-11
x 1
x 3
x 7
x 1
x 3
x 4
TUG-3
TUG-2
x 3
x 7
VC-4
VC-3
AU-4
AU-3
x 1
x 3
AUG
x N
STM-N

FIG. 3

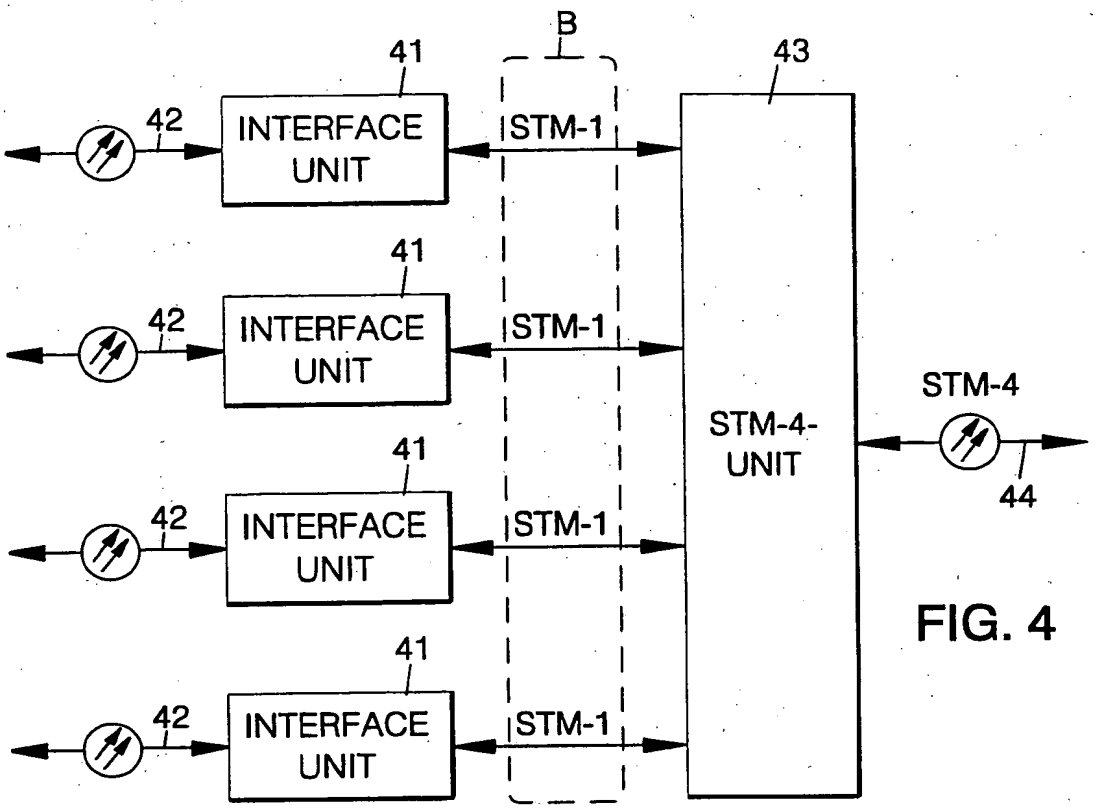
B
41
43
42
INTERFACE UNIT
STM-1
STM-4-UNIT
STM-4
44

FIG. 4

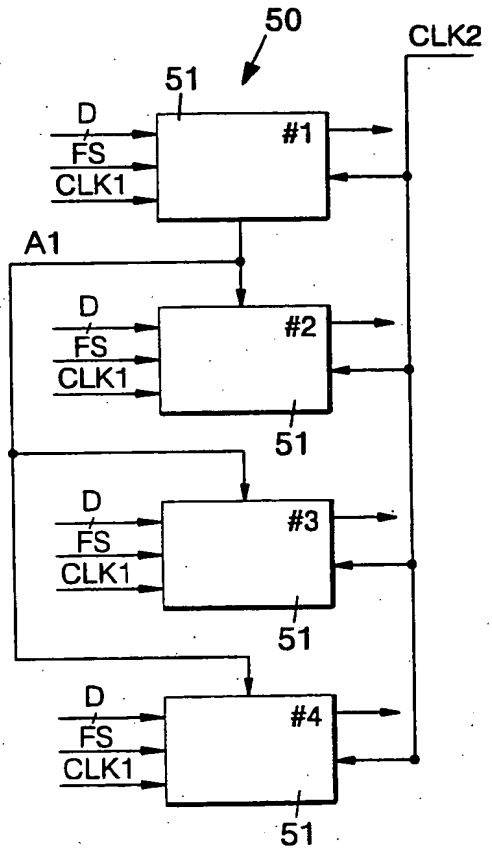
50
CLK2
51
D
FS
CLK1
#1
A1
#2
#3
#4

FIG. 5

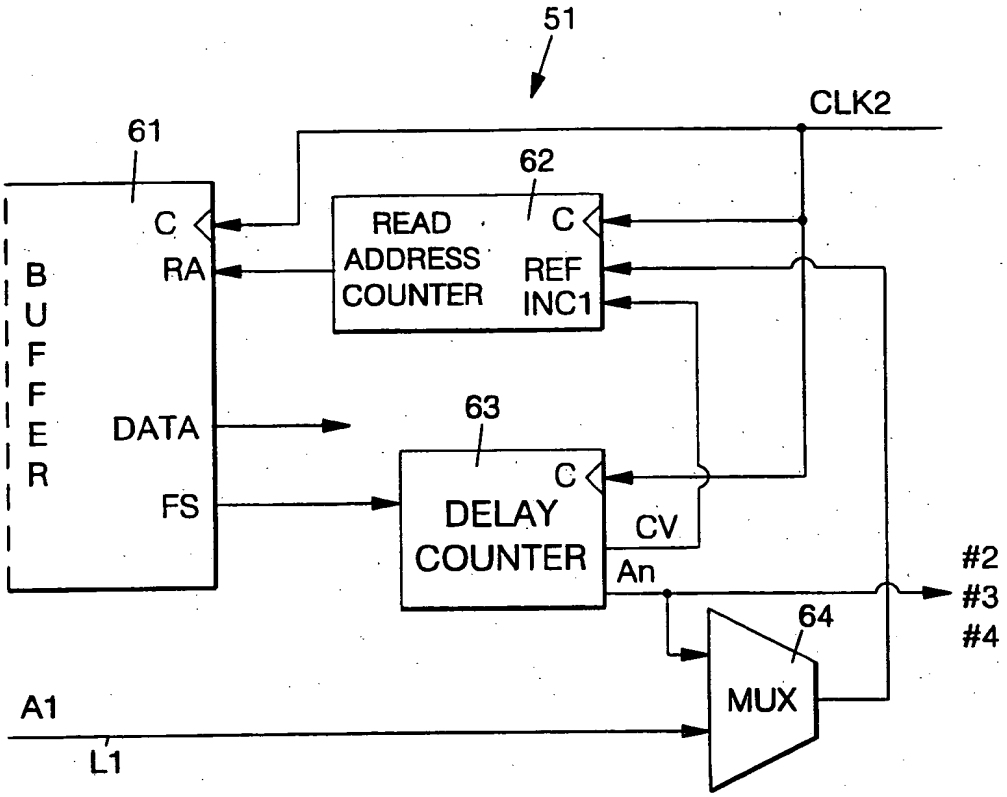
51
CLK2
61
62
C
RA
READ
ADDRESS
COUNTER
C
REF
INC1
B
U
F
F
E
R
DATA
FS
63
C
DELAY
COUNTER
CV
An
#2
#3
#4
64
MUX
A1
L1

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 94/00216

A. CLASSIFICATION OF SUBJECT MATTER

IPC 5 : H04J 3/16, H04J 3/06
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 5 : H04J, H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CLAIMS, WPI, EPODOC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4993026 (MIKIO YAMASHITA), 12 February 1991 (12.02.91), column 1, line 38 - column 2, line 36, figure 3, claim 1 --	1-9
A	US, A, 5046064 (TOSHIO SUZUKI ET AL), 3 Sept 1991 (03.09.91), abstract, see the whole document --	1-9
A	EP, A1, 0543327 (NEC CORPORATION), 26 May 1993 (26.05.93), column 2, line 19 - column 3, line 43 --	1-9
A	US, A, 5168494 (HORST MUELLER), 1 December 1992 (01.12.92), see the whole document --	1-9

[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
13 Sept 1994	16 -09- 1994
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Göran Magnusson Telephone No. +46 8 782 25 00

INTERNATIONAL SEARCH REPORT

International application No.
PCT/FI 94/00216

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 5033044 (TIMOTHY J. WILLIAMS ET AL), 16 July 1991 (16.07.91), column 4, line 26 - column 5, line 63, abstract	1-9

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INTERNATIONAL SEARCH REPORT

Information on patent family members

27/08/94

International application No.
PCT/FI 94/00216

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 4993026	12/02/91	JP-A- 2090739	30/03/90
US-A- 5046064	03/09/91	EP-A- 0380368	01/08/90
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US-A- 5168494	01/12/92	AU-B- 620744	20/02/92
		AU-A- 6706490	06/06/91
		CA-A- 2030954	30/05/91
		CN-A- 1053157	17/07/91
		EP-A- 0429888	05/06/91
US-A- 5033044	16/07/91	NONE	